WHAT IS CLAIMED IS:

1. A semiconductor device, comprising:

a fin structure comprising a semiconducting material, the fin structure including a channel stop layer;

a source region formed at one end of the fin structure, the channel stop layer separating the source region into a first source region and second source region;

a drain region formed at an opposite end of the fin structure, the channel stop layer separating the drain region into a first drain region and second drain region; and

at least one gate.

2. The semiconductor device of claim 1, wherein the channel stop layer has a retrograde channel concentration profile.

3. The semiconductor device of claim 2, wherein the retrograde channel concentration profile confines a depletion region of a junction formed between the first source region and the second source region and between the first drain region and the second drain region.

4. The semiconductor device of claim 1, wherein the channel stop layer comprises ions implanted into the fin structure at a selected concentration and at a selected implantation energy level.

5. The semiconductor device of claim 1 wherein the first source region and the first

drain region are formed on a first side of the retrograde channel stop layer and the second source region and the second drain region are formed on an opposite side of the channel stop layer.

6. The semiconductor device of claim 5, wherein the first source region and the first drain region are part of an N-channel device, and

wherein the second source region and the second drain region are part of a P-channel device.

7. The semiconductor device of claim 6, wherein each of the N-channel device and the P-channel device includes the at least one gate.

8. A semiconductor device, comprising:

a fin structure that includes a retrograde channel stop layer that extends a length of the fin structure and is positioned approximately in a center of the fin structure;

a source region formed at one end of the fin structure, the retrograde channel stop layer separating the source region into a first source region and second source region; and

a drain region formed at an opposite end of the fin structure, the retrograde channel stop layer separating the drain region into a first drain region and second drain region.

9. The semiconductor device of claim 8, wherein the retrograde channel stop layer has a retrograde channel concentration profile.

10. The semiconductor device of claim 9, wherein the retrograde channel concentration profile confines a depletion region of a junction formed between the first source region and the second source region and between the first drain region and the second drain region.

11. The semiconductor device of claim 8, wherein the retrograde channel stop layer comprises ions implanted into the fin structure at a selected concentration and a selected implantation energy level.

12. The semiconductor device of claim 8, further comprising at least one gate formed over the fin structure.

13. The semiconductor device of claim 8, wherein a width of the fin structure ranges from about 70 Å to about 80 Å.

14. The semiconductor device of claim 8, wherein the first source region and the first drain region are formed on a first side of the retrograde channel stop layer and the second source region and the second drain region are formed on an opposite side of the retrograde channel stop layer.

15. The semiconductor device of claim 14 wherein the first source region and the first drain region are part of an N-channel device, and

wherein the second source region and the second drain region are part of a P-channel device.

16. The semiconductor device of claim 8, wherein the first source and drain regions are doped with n-type impurities and the second source and drain regions are doped with p-type impurities, and

wherein the semiconductor device further comprises:

a common gate formed on at least a top and one side surface of the fin structure.

17. A semiconductor device comprising:

an N-channel device including a first source region, a first drain region, a first fin structure, and a gate; and

a P-channel device including a second source region, a second drain region, a second fin structure, and the gate, the second source region, the second drain region, and the second fin structure being separated from the first source region, the first drain region, and the first fin structure by a channel stop layer.

18. The device of claim 17, wherein the channel stop layer has a retrograde channel concentration profile.

19. The device of claim 18, wherein the retrograde channel concentration profile

confines a depletion region of a junction formed between the first source region and the second source region and between the first drain region and the second drain region.

20. The device of claim 17, wherein the channel stop layer comprises ions implanted into the semiconductor device at a selected concentration and a selected implantation energy level.